

**TIME-BASE IMPLEMENTATION FOR CORRECTING
ACCUMULATIVE ERROR WITH CHIP FREQUENCY SCALING**

ABSTRACT

The present invention provides for supporting an on
chip-timer facility and, more particularly, to the
5 generation of a constant time incremental increase while
changing core mesh-clock frequency. A latch is coupled to
the output of a first free-running clock. An inverter is
coupled to the output of the first latch. At least one
other secondary latch is coupled to the output of the first
10 latch. An edge detector is coupled to the output of the
secondary latch. An incrementer or decrements is coupled
to the output of the edge detector. A memory is coupled to
the output of the incrementer or decrements.